



Attorney Docket No. 42P4514D

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*Smiler*

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re the Patent Application of:

Brian S. Doyle

Serial No. 09/416,501

Filed: October 8, 1999

For: **METHOD FOR DELAMINATING A  
THIN FILM USING NON-THERMAL  
TECHNIQUES**

Examiner: Ortiz, Edgardo

Art Unit: 2815

**APPEAL BRIEF**

Mail Stop Appeal Brief - Patents  
Commissioner for Patents  
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Alexandria, VA 22313-1450

Dear Commissioner:

Applicant submits, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Applicant also submits herewith a check in the amount of \$320.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 1.17(c). Please charge any additional amount due or credit any overpayment to deposit Account No. 02-2666.

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Serial No. 09/416,501  
Atty. Docket No: 42P4514D



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**I. REAL PARTY IN INTEREST**

Brian S. Doyle, the party named in the caption, assigned his rights to that disclosed in the subject application through an assignment recorded on October 16, 1998 (Reel 9523/Frame 0291) to Intel Corporation, of Santa Clara, California. Thus, as the owner at the time the brief is being filed, Intel Corporation, of Santa Clara, California is the real party in interest.

**II. RELATED APPEALS AND INTERFERENCES**

There are no other appeals or interferences that will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal.

**III. STATUS OF CLAIMS**

Claims 28-31, 33, 34 and 37 are pending in the application. The Examiner has rejected all pending claims. Applicant hereby appeals the rejection of all the pending claims.

**IV. STATUS OF AMENDMENTS**

No amendment has been filed subsequent to the Final Office Action having a mailing date of February 6, 2003.

**V. SUMMARY**

An integrated circuit is disclosed that includes a first substrate having a first set of active devices formed thereon and a second substrate having a second set of active devices formed thereon. (Specification, p. 11, line 9 to p. 13, line 22). The first substrate is coupled to the second substrate such that selected ones of the first set of active devices of the first substrate are intercoupled via metal lines to selected ones of the second set of active devices of the second substrate. (Specification, p. 13, lines 9-16).

**VI. ISSUES**

The issue involved in this appeal is as follows:

Under 35 U.S.C. § 103(a), are Claims 28-31, 33, 34 and 37 obvious over Yonehara et al. (U.S. Patent No. 6,150,031) in view of FIG. 2 of Applicant's specification)?

## **VII. GROUPING OF CLAIMS**

Applicant contends that the claims can be divided into three groups and that each group of claims is separately patentable. These groups are as follows:

- Group I - Claims 28 and 29
- Group II - Claim 30
- Group III - Claims 31, 33, 34 and 37

The claims of Groups I through III are apparatus claims. Each claim group is deemed separately patentable for the reasons given below.

## **VIII. ARGUMENT**

### **A. Overview of the Cited Reference**

#### **1. Overview of Yonehara**

Yonehara describes a process of obtaining a semiconductor substrate by making porous all of a silicon monocrystalline substrate and permitting a monocrystalline layer to be epitaxially grown. (Yonehara, col. 10, lines 25-28). Figure 1A of Yonehara shows a monocrystalline layer (22) formed on a first silicon substrate (21). (Yonehara, col. 10, lines 29-39). Figure 1B of Yonehara shows a second silicon substrate (23) having an oxidized layer (24) formed on its surface, which is bonded onto the surface of the monocrystalline layer (22). (Yonehara, col. 10, lines 40-44). Figure 1C of Yonehara shows the first silicon substrate (21) etched away such that the monocrystalline layer (22) remains on the oxidized layer (24). (Yonehara, col. 10, lines 44-47). Absent from Yonehara is any teaching or suggestion of active devices formed on the monocrystalline layer (22), much less intercoupling selected ones of the active devices via metal lines.

### **B. Group I: Rejection Of Claims 28 And 29 Under 35 U.S.C. §103(a) As Being Obvious Over Yonehara In View Of Fig. 2 Of Applicant's Specification**

The Examiner rejects Claims 28 and 29 under 35 U.S.C. § 103(a) as being unpatentable over Yonehara in view of FIG. 2 of Applicant's specification.

Claim 28 recites an apparatus comprising:

- [1] a first substrate portion having a dielectric layer on a surface; and
- [2] a second single crystal substrate portion defining a device surface wherein the dielectric layer of the first substrate portion is bonded directly to the device surface of the second substrate portion,

[3] the second single crystal substrate having active devices formed thereon,

[4] wherein selected ones of said active devices of said second substrate portion are intercoupled via metal lines.

In rejecting Claim 28, the Examiner asserts that Yonehara teaches limitations [1] and [2] of Claim 28 but fails to teach limitations [3] and [4]. The Examiner asserts that limitations [3] and [4] of Claim 28 are taught by FIG. 2 of Applicant's specification.

Applicant respectfully submits that Claim 28 is not obvious over Yonehara in view of FIG. 2 of Applicant's specification. Specifically, neither Yonehara nor FIG. 2 teaches or suggests a dielectric layer of a first substrate portion bonded directly to a device surface of a second substrate portion having active devices formed thereon, as recited in Claim 28. FIG. 2 of Applicant's specification merely notes that, prior to the disclosure, it was not possible to fabricate a second layer of active devices made of single silicon crystal because the active devices and/or metal lines interconnecting the active devices will become damaged during the fabrication process. Yonehara adds nothing to FIG. 2 of Applicant's specification since it merely teaches forming a monocrystalline layer on a surface of a porous silicon layer without addressing the problem of fabricating a second layer of active devices made of single silicon crystal without damaging the active devices and/or the metal lines interconnecting the active devices. In fact, there is nothing in Yonehara that teaches or suggests forming active devices on the second single crystal substrate portion, much less intercoupling selected ones of the active devices of the second substrate portion via metal lines.

Yonehara discloses a first substrate portion 23 having a dielectric layer 24 and a second single crystal substrate 22 formed on the dielectric layer 24. However, as correctly noted by the Examiner, Yonehara does not teach or suggest a second single crystal substrate portion having active devices formed thereon and defining a device surface, as required by Claim 28. Additionally, as correctly noted by the Examiner, Yonehara does not teach or suggest intercoupling selected ones of the active devices of the second substrate portion via metal lines, as required by Claim 28.

Applicant submits that FIG. 2 of Applicant's specification also does not disclose or suggest a second single crystal substrate portion having active devices formed thereon and intercoupled via metal lines, as required by Claim 28. Instead, the background section and FIG. 2 of Applicant specification merely mention that, prior to the disclosure, the second layer of active devices (transistors) was not made of a single-crystal silicon but was made of a polycrystalline silicon or amorphous silicon because fabrication of a second layer of active devices made of single silicon crystal requires processing steps that are performed well beyond the temperature that the interconnect system (e.g., metal lines interconnecting the transistors) can withstand.

In this regard, it is not clear how the structure taught by Yonehara could be modified in accordance with the subject matter of Claim 28 because neither Yonehara nor FIG. 2 discloses or suggests that it is possible to fabricate a second layer of active devices made of single silicon crystal with metal lines intercoupling the active devices. Therefore, Applicant submits that, even if Yonehara and FIG. 2 could be combined, the combination would not yield the apparatus as claimed in Claim 28, as neither Yonehara nor FIG. 2 disclose or suggest providing a second single crystal substrate portion having active devices formed thereon in which the active devices are intercoupled via metal lines. Accordingly, Yonehara and FIG. 2, individually or in combination, fail to disclose or suggest providing a second single crystal substrate portion having active devices formed thereon in which the active devices are intercoupled via metal lines, as claimed in Claim 28.

Moreover, Applicant respectfully submits that the obviousness rejection of Claim 28 is based on impermissible hindsight analysis. More specifically, because the reference (Yonehara) relied upon by the Examiner does not relate to the same problem confronted by the inventor, Applicant submits that the obviousness rejection of Claim 28 is based on an impermissible hindsight analysis.

When an obviousness rejection is made based upon a combination of references, the Examiner “must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed.” In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998). Moreover, it is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior or by implications contained in such teachings or suggestions. In re Sernaker, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). In addition, the Federal Circuit states that “[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.” In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), citing In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

As noted above, the Federal Circuit requires that the Examiner’s basis for combining the references relates to the same problem as that confronted by the inventor. One of the problems that the patent application and the claimed subject matter addresses is making an integrated circuit smaller by reducing the X-Y dimensions of the integrated circuit. In accordance with one embodiment, the patent application provides a way to further reduce the X-Y dimensions of an integrated circuit by providing a second level of transistors in the Z dimension made of a single crystal. However, Yonehara does not relate to reducing X-Y dimensions of an integrated circuit by providing a second level of transistors in the Z dimension. In fact, there is nothing in Yonehara that

discloses or suggests that the second layer made of single silicon crystal may be used to reduce the X-Y dimensions of an integrated circuit by providing a second level of transistors in the Z dimension. Because Yonehara relied upon by the Examiner does not address to the same problem confronted by the inventor, Applicant respectfully asserts that the obviousness rejection of Claim 28 is based on an impermissible hindsight analysis.

Furthermore, in rejecting Claim 28, the Examiner is unable to point out any specific teaching or suggestion for combining Yonehara with FIG. 2. The Examiner is instead relying on what it presumes is the level of knowledge of one of ordinary skill in the art at the time of the invention to supply the missing suggestion to combine. However, the one of ordinary skill in the art component will rarely operate to supply missing knowledge and to support a suggestion or motivation to combine references. See Al-Site Corp. v. VSI International, Inc., 174 F.3d 1308, 1324 (Fed. Cir. 1999). See W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983) (holding that “[t]o imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher”); Ryko Mfg. Co. v. Nu-Star, Inc., 950 F.2d 714, 718, 21 USPQ2d 1053, 1057 (Fed. Cir. 1991) (holding that one of ordinary skill in the art does not act as a bridge over gaps in substantive presentation of an obviousness case). Accordingly, Applicant respectfully asserts that the obviousness rejection of Claim 28 is based on an impermissible hindsight analysis.

In view of the foregoing, Applicant submits that the rejection of Claim 28 under 35 U.S.C. §103(a) is in error.

Claim 29 is dependent on patentably independent Claim 28, as discussed above, and those arguments are hereby incorporated regarding Claim 29. At least for this reason, Applicant submits that the rejection of Claim 29 under 35 U.S.C. §103(a) is in error.

**C. Group II: Rejection Of Claim 30 Under 35 U.S.C. §103(a) As Being Obvious Over Yonehara In View Of FIG. 2 Of Applicant's Specification**

The Examiner rejects Claim 30 under 35 U.S.C. § 103(a) as being unpatentable over Yonehara in view of FIG. 2 of Applicant's specification.

In rejecting Claim 30, the Examiner asserts that “a further difference between the claimed invention and Yonehara is, selected ones of the devices of the first substrate portion and selected ones of the devices of the second substrate portion that are interconnected. Applicant's admitted prior art figure 2 teaches selected ones of the first level of devices (204) of the primary substrate (202) and selected ones of the devices (203) of the secondary substrate (Si) that are interconnected.

Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Yonehara to include selected ones of the devices of the first substrate portion and selected ones of the devices of the second substrate portion that are interconnected, in order to improve the integration and bonding of semiconductor layers including transistors.”

Claim 30 is dependent on patentably independent Claim 28, as discussed above, and those arguments are hereby incorporated regarding Claim 30.

Additionally, Applicant respectfully submits that Claim 30 is not obvious over Yonehara in view of FIG. 2 of Applicant’s specification. Specifically, the structure taught by Yonehara cannot be modified in accordance with the subject matter of Claim 30 because neither Yonehara nor FIG. 2 provides a way to fabricate multiple layers of active devices, in which the second single crystal substrate includes active devices formed thereon, without damaging the active devices and/or the metal lines intercoupling the active devices during the fabrication process. Accordingly, even if Yonehara and FIG. 2 could be combined, the combination would not yield the apparatus as claimed in Claim 30, as neither Yonehara nor FIG. 2 teaches how to fabricate multiple layers of active devices without damaging the essential components (i.e. active devices and metal lines intercoupling the active devices) during the fabrication process.

If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). In this case, even if the structure taught by Yonehara could be modified as suggested by the Examiner, such proposed modification would render the structure of Yonehara unsatisfactory for its intended purposes, because active devices and/or metal lines formed in the monocrystalline layer (22) would become damaged during the fabrication process. Since the proposed modification would render the structure of Yonehara unsatisfactory for its intended purposes, Applicant submits that there is no suggestion or motivation to make the proposed modification.

In view of the foregoing, Applicant submits that the rejection of Claim 30 under 35 U.S.C. §103(a) is in error.

**D. Group III: Rejection Of Claims 31, 33, 34 And 37 Under 35 U.S.C. §103(a) As Being Obvious Over Yonehara In View Of FIG. 2 Of Applicant’s Specification**

The Examiner rejects Claims 31, 33, 34 and 37 under 35 U.S.C. § 103(a) as being unpatentable over Yonehara in view of FIG. 2 of Applicant’s specification.



In rejecting Claim 31, the Examiner asserts that “Yonehara teaches a primary substrate (23) and at least a secondary single crystal substrate (22) coupled to the primary substrate” but “fails to teach devices formed on the primary substrate and the secondary substrate, wherein devices surfaces of the primary and secondary substrate are connected directly such that selected active devices of the second single crystal substrate [are] intercoupled via metal lines to selected ones of the first level of devices of the primary substrate.” The Examiner further asserts that the limitations “wherein the first device surface of the primary substrate is connected directly to the second device surface of the at least one secondary single crystal substrate such that selected ones of said active devices of said at least one secondary single crystal substrate are intercoupled via metal lines to selected ones of the first level of devices of the primary substrate” are taught by FIG. 2 of Applicant’s specification.

Applicant respectfully submits that Claim 31 is not obvious over Yonehara in view of FIG. 2 of Applicant’s specification. Specifically, the structure taught by Yonehara cannot be modified in accordance with the subject matter of Claim 31 because neither Yonehara nor FIG. 2 provides a way to fabricate multiple layers of active devices, in which the at least one secondary single crystal substrate includes active devices formed thereon, without damaging the active devices and/or the metal lines intercoupling the active devices during the fabrication process. Accordingly, even if Yonehara and FIG. 2 could be combined, the combination would not yield the apparatus as claimed in Claim 31, as neither Yonehara nor FIG. 2 teaches how to fabricate the apparatus claimed in Claim 31 without damaging the essential components (i.e. active devices and metal lines intercoupling the active devices) during the fabrication process.

If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). In this case, even if the structure taught by Yonehara could be modified as suggested by the Examiner, such proposed modification would render the structure of Yonehara unsatisfactory for its intended purposes, because active devices and/or metal lines formed in the monocrystalline layer (22) would become damaged during the fabrication process. Since the active devices and metal lines formed in the monocrystalline layer (22) would become damaged during the fabrication process, Applicant respectfully submits that there is no suggestion or motivation to make the proposed modification.

Furthermore, Applicant respectfully submits that the obviousness rejection of Claim 31 is based on impermissible hindsight analysis. As noted above, because Yonehara relied upon by the Examiner does not relate to the same problem confronted by the inventor, Applicant submits that the obviousness rejection of Claim 31 is based on an impermissible hindsight analysis.

In view of the foregoing, Applicant submits that the rejection of Claim 31 under 35 U.S.C. §103(a) is in error.


Claims 33, 34 and 37 are dependent on patentably independent Claim 31, as discussed above, and those arguments are hereby incorporated regarding Claims 33, 34 and 37. At least for this reason, Applicant submits that the rejection of Claims 33, 34 and 37 under 35 U.S.C. §103(a) is in error.

**IX. CONCLUSION AND RELIEF**

Based on the foregoing, Applicant requests that the Board overturn the rejection of all pending claims and hold that all of the claims of the present application are allowable.

Respectfully submitted,  
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

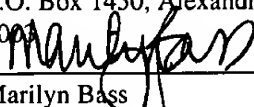
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\_\_\_\_\_  
Marilyn Bass

May 20, 2003

**X. APPENDIX**

The claims involved in this Appeal are as follows:

1-27. (Canceled)

28. (Previously Amended) An apparatus comprising:  
a first substrate portion having a dielectric layer on a surface; and  
a second single crystal substrate portion having active devices formed thereon and defining a device surface wherein the dielectric layer of the first substrate portion is bonded directly to the device surface of the second substrate portion, wherein selected ones of said active devices of said second substrate portion are intercoupled via metal lines.

29. (Previously Added) The apparatus of claim 28, further comprising a plurality of devices formed on the first substrate portion.

30. (Previously Added) The apparatus of claim 29 wherein selected ones of the devices of the first substrate portion and selected ones of the devices of the second substrate portion are interconnected.

31. (Previously Amended) An apparatus comprising:  
a primary substrate having a first level of devices formed thereon and defining a first device surface; and  
at least one secondary single crystal substrate having active devices formed thereon and defining a second device surface, wherein the first device surface of the primary substrate is connected directly to the second device surface of the at least one secondary single crystal substrate such that selected ones of said active devices of said at least one secondary single crystal substrate are intercoupled via metal lines to selected ones of the first level of devices of the primary substrate.

32. (Canceled)

33. (Previously Added) The apparatus of claim 28, wherein said first substrate portion is made of a single crystal silicon.

34. (Previously Added) The apparatus of claim 31, wherein said primary substrate is made of a single crystal silicon.

35-36. (Canceled)

37. (Previously Added) The apparatus of claim 28, wherein the first substrate portion is formed as a film of less than an entire portion of a starting material by demarcating a film thickness through an ion implantation into the starting material and separating the first substrate portion from the starting material.